CONSIDERATIONS ON SWITCHING LOSSES IN HIGH FREQUENCY ZVS CONVERTERS

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Abstract. *In ZVS converters, switches are automatically turned on when their voltages are zero, and are forced to turn off at a desired time, to achieve regulation. Since the switch voltage is zero when turning on, a simple snubber may be placed across each switch to take over switch conduction during turning off. This allows zero turn-off (and turn-on) losses to be achieved, with reduced EMI. Significant additional losses and EMI reductions can be made with oversized FET switches or several paralleled FET switches, where the non-linear FET output capacity serves as a commutation capacity.*

Keywords: *converter, losses, commutation, driver*

Introduction

Very low switching losses can be achieved in several classes of power converters, using various resonant and quasi-resonant modes of operation. The Zero Voltage Switching (ZVS) is a resonant transition mode approach, also sometimes termed "thyristor dual". Switch turn-on is practically "automatic", when the switch voltage falls to zero, and the turn-off is forced (this is the "dual" of conventional thyristors, where turn-on is forced and turn-off is automatic, when the current falls to zero).

Usually, the switches are paralleled with snubber or commutation capacitors to take over conduction upon turn-off, resulting in zero turn-off losses. The zero voltage at turn on is typically achieved with stored inductive energy, when another switch is turned off. Many variable frequency resonant converters operate in this mode.

The thyristor dual mode can be achieved in some more-or-less conventional converter topologies, with constant frequency operation, possible in some topologies with two or more active switches. The phase-shifted bridge with four switches is a common example. Some types of single ended forward and fly-back converters can also be operated in the thyristor dual mode, when an active transformer reset circuit is used. In many of these, the minimal switching losses characteristics of resonant converters are combined with the low conduction losses of classical "hard-switched" Pulse Width Modulated - PWM topologies.

Hard commutation thyristor dual converters

A simple half-bridge thyristor dual converter is shown for illustration in Figure 1. The inductor L_1 provides the commutation energy to charge and discharge C_1 and C_2 during the switching process. The impedance Z represents the rest of the converter, and may include other reactive elements (an output transformer and filters). In a simple half bridge circuit Z=0. The extremely high efficiency reachable with the circuit, can be used to measure the magnetic core losses in L_1, from the DC input power. This type of converter has essentially zero switching losses and a relatively smooth linear voltage transition during the switching interval, which helps to reduce some sources of EMI (mainly, conducted common mode noise).

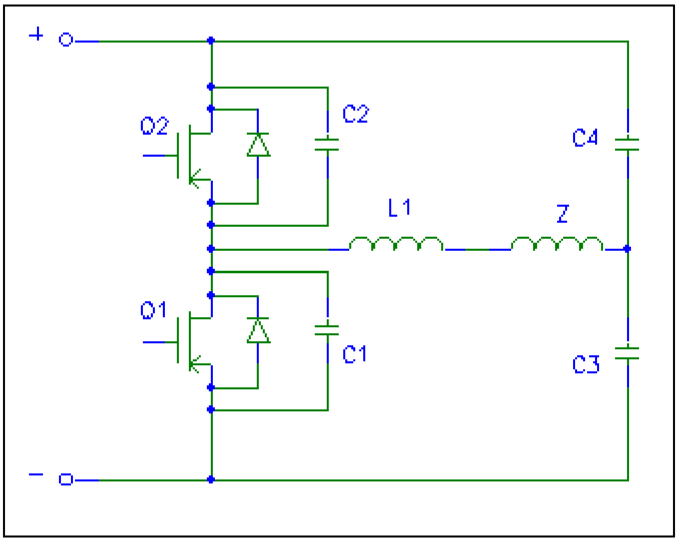

FIGURE 1. A typical "thyristor dual" converter

Relatively high dI/dt current transitions remain however, and can contribute to radiated EMI (inductively coupled to common and normal mode conducted noise in poor circuits layout design).

This could be is illustrated in the idealised test circuit of Figure 2, witch models the operation of the Figure 1 circuit during the turn-off of Q_1.

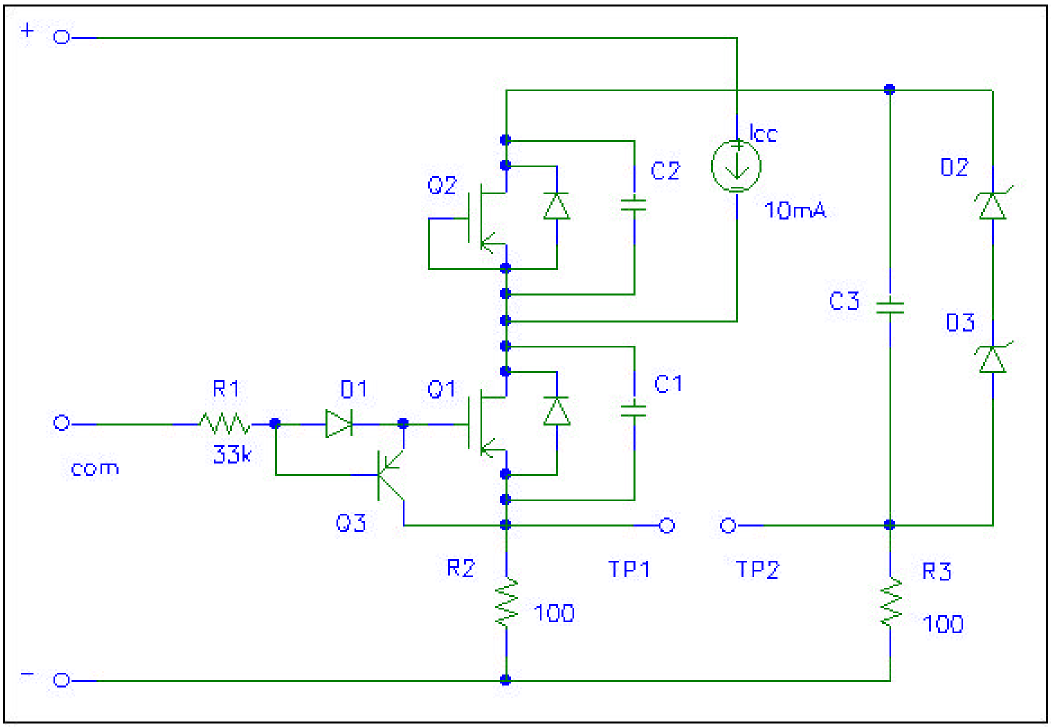

FIGURE 2. The thyristor dual commutation test circuit

When Q_1 turns off, the 10mA current that was flowing in Q_1, now splits between the snubber capacitors C_1 and C_2 during the voltage transition, as shown in the scope plot (Figure 3). The current diverts from C_1 and C_2 to Q_2 when the body-drain diode of Q_2 becomes forward biased. As can be seen, relatively sudden current transitions occur at the beginning and at the end of the switching transition.

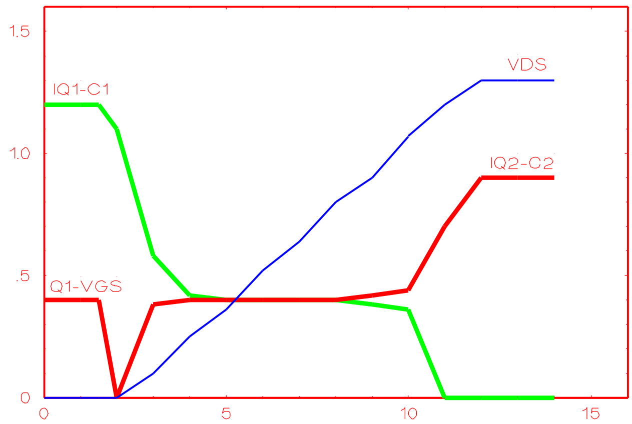

FIGURE 3. “Hard” current commutation

Practically, the situation is even less ideal, because C_1 and C_2 cannot be physically in the same place as Q_1 and Q_2; there will be some parasitic inductance in the Q_1-C_1 and Q_2-C_2 loops. Thus when Q_1 turns off, the current must first flow to the physically separate paths through C_1 and C_2, which introduces some ringing in current waveforms. A similar ringing will occur when C_1 and C_2 currents are suddenly switched to Q_2. These ringing currents are difficult to dampen, and contribute to radiated EMI.

Soft commutation thyristor dual converters

In soft commutation thyristor dual converters, the current commutation becomes much smoother, with significantly reduced EMI, when large or more small paralleled FETs are used without additional commutation capacitors. FET output capacity is strongly voltage dependent, as shown in Figure 4 (i.e. for IRF740 - V_{DSmax} = 400V). The output capacity drops by about 40:1 as the drain-source voltage V_{DS} raises from 1V to several hundred volts.

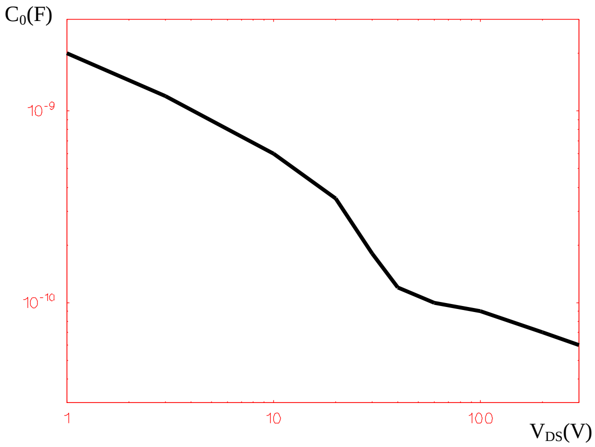

Figure 4. Typically C_o vs. V_{DS} for an IRF740 FET

The reduction of dI/dt is illustrated by replacing the commutation capacitors C_1 and C_2 (440pF) in Figure 2 with three paralleled FETs (IRF740), in order to obtain the same total commutation capacity. Now, when Q1 turns off, the capacity across Q_1 is about 40 times larger than across Q_2, and about 97% of the current initially continue to flow through Q_1. The Q_1 capacity falls and the Q_2 capacity raises as well as the Q_1 drain voltage, causing the current to gradually switch from Q_1 to Q_2.

A less obvious benefit is that a FET output capacity is in the same volume as the ohmic conduction, and thus the snubber capacity currents flow through the same physical paths as the switch conduction currents. There is practical no discontinuity in the power current flow in either time or space, and high frequency EMI due to changing magnetic fields is reduced to its minimum possible value. Since these ideal snubber capacitors are made with the use of large FETs, conduction losses are also reduced. Combined switching and conduction “chopper” losses may often be reduced to less than 1% of output power if desired, and losses less than 0.1% of output power.

The only negative effect of this technique is the high cost of the oversized active switches. Less important is the drive loses that are higher than in standard schemes.

References

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