NEW RESONANT CIRCUIT FOR ZERO VOLTAGE SWITCHING AT THE POWER CONVERTERS

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Abstract

This paper presents a new resonant circuit meant to switch the solid state devices by ZVS at the power converters. This resonant circuit is characterized by a low clamping ratio K (between 1.15 and 1.20) and a small total duration of its operation.

1. Introduction

During the last years, important research efforts have been performed to elaborate converters with resonant circuits in which the solid state devices is performed at zero voltage (ZVS) or zero current (ZCS).

A power converters with resonant circuit acting according to this principle has the following advantages.

-the devices switching losses at both turning off/on vanish, offering the converter a high efficiency.

-the electromagnetic interference (EMI) problems are less severe since the resonance pulses have dv/dt smaller than for a hard switched converter.

-the converter can be operated without snubbers at the solid state devices.

The version presented in fig.1a represents a resonant circuit with constant voltage applied across the clamp capacitor. This is with non-permanent operation and is characterized by a small clamping ratio (K=1.15 ÷ 1.20). In the following we shall present its operating principle and its main characteristics.

2. The operating principle of the resonant circuit with constant voltage applied on the clamp capacitor

The operation of the resonant circuit with reduced clamping ratio and constant voltage across the clamp capacitor, presented in fig. 1a, consists of 4 stages.

- First stage: the clamp capacitor discharging through the inductance L.

The discharge of the capacitor C_c", with a large capacity, on the inductance L is performed at constant voltage $(K - 1)V_d$ when the tranzistor T_c turns-on. Though the tranzistor T_r turns-on at the same time with T_c, the voltage v_r remains in the first stage equal to KV_d, since the voltage on C_c" is practically kept constant. All along this stage it is supposed that the load current i_d is also constant, namely it equals I_d'. It is admitted that during the duration t_1 of this stage, the current through C_c" increases from zero to I_{max}, and the current trough L changes linearly from I_d' to $(I_d' - I_{max}) = - I_{L1} < 0$ (fig.2.a).

$$(K-1)\,V_d = L\frac{I_{cmax}}{t_1} = L\frac{I_d+I_{L1}}{t_1} \qquad (1)$$

The voltage v_i applied at the output in the first stage keeps constant, namely $v_r = KV_d$, and the value I_d' can be positive, zero or negative.

- Second stage: the discharge of the capacitor C_r.

In this stage the tranzistor T_r remains in conduction, and T_c turns-off. At the output on applies the voltage $v_r = v_i$ which decreases from KV_d to zero. The current i_L through the inductance L, and the voltage v_r given by the relations:

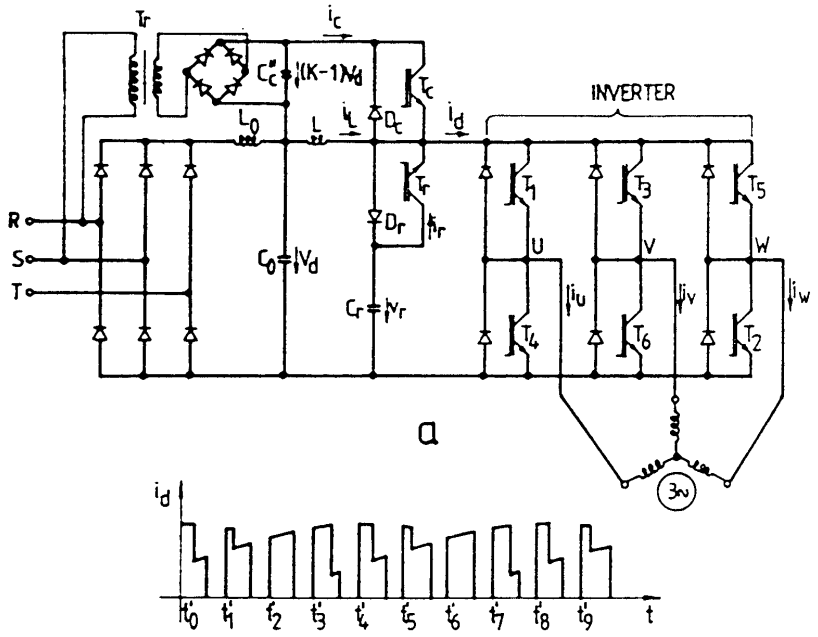
Tr
i_c
C_c'' ↕(K-1)V_d
T_c
INVERTER
L_0
L
i_L
D_c
i_d
T_r
D_r
i_r
R
S
T
C_0 ↕V_d
C_r ↕V_r
T_1
T_3
T_5
U
V
W
T_4
T_6
T_2
i_u
i_v
i_w
3~
a
i_d
t_0' t_1' t_2' t_3' t_4' t_5' t_6' t_7' t_8' t_9' t
b

Fig. 1

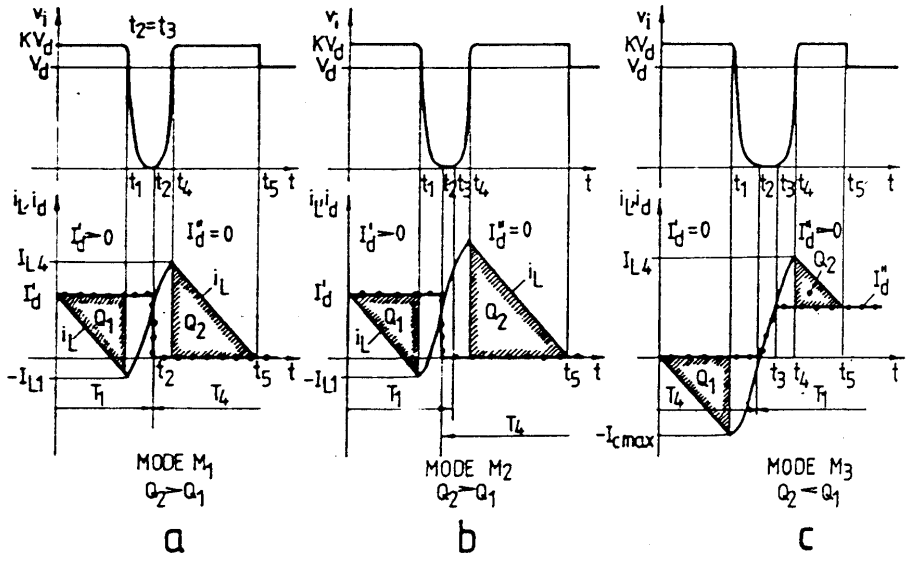
v_i
KV_d
V_d
$t_2=t_3$
t_1 t_2 t_4 t_5 t
i_L i_d
$I_d'=0$
$I_d''=0$
I_{L4}
I_d'
i_L
Q_1
Q_2
$-I_{L1}$
T_1
T_4
MODE M_1
$Q_2>Q_1$
a
t_3
$I_d'>0$
MODE M_2
$Q_2>Q_1$
b
$I_d'=0$
$I_d''>0$
$-I_{cmax}$
MODE M_3
$Q_2=Q_1$
c

Fig. 2

$$i_L = -(K-1)V_d\sqrt{\frac{C_r}{L}}\sin\omega_o(t-t_1) - I_{cmax}\cos\omega_o(t-t_1) + I_d \quad (2)$$

$$v_r = (K-1)V_d\cos\omega_o(t-t_1) - I_{cmax}\sqrt{\frac{L}{C_r}}\sin\omega_o(t-t_1) + V_d \quad (3)$$

where the rezonant pulsation ω_o is given by:

$$\omega_o = \frac{1}{\sqrt{LC_r}} \quad (4)$$

The second stage has a duration $(t_2 - t_1)$ and at its end the voltage on the capacitor C_r vanishes. After simple calculations the value I_{L2} of the current passing through L at the end of the second stage results:

$$I_{L2} = I_d - \sqrt{I^2_{cmax} - K(2-K)\frac{C_r}{L}V^2_d} \quad (5)$$

and the duration $(t_2 - t_1)$ is obtained from the relation:

$$\cos\omega_o(t_2-t_1) = \frac{-1+(\omega_o t_1)\sqrt{(K-1)^2(\omega_o t_1)^2 - K(2-K)}}{(K-1)[(\omega_o t_1)^2 + 1]} \quad (6)$$

By annuling the voltage on the C sub r element, zero voltage switching (ZVS) can be performed of the semiconductor devices (GTO, IGBT, a.s.o.) composing the power converter connected in paralel on the DC side. Aftre performing these switchings, the current i_L changes its value from I'_d to I''_d the last one being positive, zero or negative.

Third stage: keeping a zero voltage across the capacitor C_r as long as the current $(i_L - i''_d)$ is negative.

This current closes through the power converter semiconductor devices. The duration of the third stage is $(t_3 - t_2)$.

If at the moment t_2 the difference $(I_{L2} - I''_d)$ is positive, the switchings of the semiconductor devices can be performed, and the duration of the third stage is zero, accordind to Fig. 2.a (hence $t_2 = t_3$). For example, in the case of the inverter presented in Fig 1.a, at the moment $t_2 = t_3$ the tranzistor T_1 can turn off and the tranzistor T_4 turns on. This can be labelled as the M_1 operating mode.

Yet, if during the short $(t_3 - t_2)$ time interval the transistors T_1 and T_4 remaind turned on, the duration of the third stage no longer vanishes, even if the difference $(I_{L2} - I''_d)$ is positive, and in this case an auxiliary energy chargind of the inductance L from the capacitor C_o occurs. This auxiliary energy will be delivred to the capacitor at the end of the fourth stage. This operating mode can be labelled as M_2 mode and is indicated in Fig.2.b

Finally, if the differnce $(I_{L2} - I''_d)$ is negative, the current through L linearly increases up to the value $I_{L3} = 0$ until the moment t_3, when the semiconductor devices switchings can be performed. This last case is indicated in Fig. 2.c and is labelled as M_3 operating mode. The hachured areas that are practically triangles, represents in order: Q_1 - the electric charge lost by the capacitor C''_o, and Q_2 - the electric charge received by this capacitor at the end of the fourth stage.

Fourth stage: chargind the capacitor C_r after performing the switchings in the power converter and after the current $(I_L - I''_d)$becomes positive.

The fourth stage lasts a time $(t_4 - t_3)$, at the moment t_4 the voltages on the capacitor C_r reaching the value KV_d. In this case, the value of the current i_L between t_3 and t_4 is given by the relation:

and the volage v_r is:

At the end of the fourth stage, the voltage v_r equals KV_d and therfore the courent i_L reaches the value:

After this stage ends, the current through L decreases from the value I_{L4} to I''_d, the energy contained in the L

$$i_L = V_d\sqrt{\frac{C_r}{L}}\sin\omega_o(t-t_3) + I_{L3}\cos\omega_o(t-t_3) \quad (7)$$

$$v_r = V_d - V_d\cos\omega_o(t-t_3) + I_{L3}\sqrt{\frac{L}{C_r}}\sin\omega_o(t-t_3) \quad (8)$$

$$I_{L4} = \sqrt{I^2_{L3} + K(2-K)\frac{C_r}{L}V^2_d} = \sqrt{I^2_{L3} + I^2_{cain}} \quad (9)$$

element being delivred to the capacitor C^*_c.

From the relation (9) one can draw the conclusion that, if $I_{L3} > I^*_c$ accordind to Figs. 2. a and b, then the energy received by element C^*_c at the end of fourth stage, from the inductance L will be larger than the energy delivred by C^*_c to L in the first stage (hence $Q_2 > Q_1$). While if $I_{L3} = I^*_c$, according to Fig.2 c, then the energy received by C^*_c at the end of the fourth stage from the element L will be smaller than the energy delivred by C^*_c to L during the first stage (hence $Q_2 < Q_1$)

In the steady operating regime of the power converter, the energy required by the capacitor C^*_c practically vanishes (hence $i_c = 0$ in Fig. 1.a), if the M_2 and M_3 operating modes are used.

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